Memory Type	Access Unit (bytes)	Relative Access Time	Special Features
local	4	1	accessed using the LM_ADDR registers
Scratch	4	10	synchronization via atomic read-modify-write support for IPC (rings) push/pull reflector mode
SRAM	4	14	follows QDR specification atomic operations support for queues and rings bit manipulation
DRAM	8	20	connects to: Xscale, microengines, and PCI bus master

Figure 17.9 Characteristics of the four primary memory types an Intel IXP2xxx uses, including relative access times measured in basic microengine instruction cycles. Although local memory can be accessed in a single cycle, three additional cycles are required to set up or change the address.