Quantity	Component	Purpose
1	Embedded RISC processor	Control, higher layer protocols, and exceptions
6	Packet processing engines	I/O and basic packet processing
1	SRAM access unit	Coordinate access to the external SRAM bus
1	SDRAM access unit	Coordinate access to the external SDRAM bus
1	IX bus access unit	Coordinate access to the external IX bus
1	PCI bus access unit	Coordinate access to the external PCI bus
several	Onboard buses	Internal control and data transfer