Processor Or Unit	Purpose
Pattern processing engine	Perform pattern matching on each packet
Queue engine	Control packet queueing
Checksum/CRC engine	Compute checksum or CRC for a packet
ALU	Conventional operations
Input interface and framer	Divide incoming packet into 64-octet blocks
Data buffer controller	Control access to external data buffer
Configuration bus interface	Connect to external configuration bus
Functional bus interface	Connect to external functional bus
Output interface	Connect to external RSP chip

Figure 15.3 Examples of functional units and processors on the Agere FPP chip. The internal bus allows processors to coordinate.