<table>
<thead>
<tr>
<th>Quantity or Size</th>
<th>Item</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IXP1200 network processor (232MHz)</td>
</tr>
<tr>
<td>8</td>
<td>Mbytes of SRAM memory</td>
</tr>
<tr>
<td>256</td>
<td>Mbytes of SDRAM memory</td>
</tr>
<tr>
<td>8</td>
<td>Mbytes of Flash ROM memory</td>
</tr>
<tr>
<td>4</td>
<td>10/100 Ethernet ports</td>
</tr>
<tr>
<td>1</td>
<td>Serial interface (console)</td>
</tr>
<tr>
<td>1</td>
<td>PCI bus interface</td>
</tr>
<tr>
<td>1</td>
<td>PMC expansion site</td>
</tr>
</tbody>
</table>

**Figure 21.1** Hardware facilities on Intel’s testbed system. The board is designed to allow engineers to evaluate a network processor.